REMARKS

The present invention is an assembly of a ground plane and a semiconductor chip, a method of assembly of a ground plane and a semiconductor chip mounted on a supporting member and a semiconductor chip package. In accordance with the invention, an assembly of a ground plane and a semiconductor chip 1 in accordance with the invention includes at least one first capacitor plate 1' within the chip 1 and at least one second capacitor plate 3 which is electrically conductive glue and further serves the purpose of attaching chip 1 to the interposer or lead frame 4. The Substitute Specification teaches respectively in paragraphs [0018] and [0020], that "all current carrying parts within the chip are considered as forming capacitor plates" and "because the electrically conductive glue defines the capacitor plate vis-à-vis the internal parts [the other capacitor plate]." The first and second capacitor plates, which respectively are the internal conductive parts 1' of chip 1 and the electrically conductive glue 3, are separated by dielectric layer 2 which may be silicon dioxide and are capacitively coupled to each other via the dielectric layer 2. The grounding plane comprises at least one first conducting member 5 and at least one electrically conductive via 7 extending through the supporting member 4 and electrically coupled in series with the second capacitor plate which is the conductive glue. This construction has numerous advantages. See paragraphs [0021]-[0024] of the specification.

Submitted herewith are new drawings addressing the issues raised by the Examiner. With respect to Section 3, new Fig. 1 contains appropriate crosshatching and further shows the internal parts of the chip 1 in a schematic

fashion which form the first capacitor plate which is identified by reference numeral 1' as described in paragraph [0018].

It is noted that the Examiner states that "[f]urthermore, the via needs to be shown to be: 'electrically coupled in series with the second capacitor plate'. " In fact, that structure is shown in Fig. 1 in that the second capacitor plate constitutes the conductive glue 3 and the vias 7 are in series therewith when the spatial relationship of the capacitor and the inductance of the vias is considered.

The Examiner has indicated that the dielectric layer recited as an integral part of the chip in claims 24 and 25 is not shown. The dielectric layer is identified by reference numeral 2 which can be seen to be an integral part of the chip 1.

The Examiner has required the layer of conductive glue to be shown between the metallic layer and the dielectric layer. In Fig. 1, the metallic layer is identified by reference numeral 5 and the dielectric layer is identified by reference numeral 2. The specification describes the layer 3, which is therebetween, as electrically conductive glue. Accordingly, it is submitted that these elements are shown in the drawings.

Section 4 sets forth various claim objections. These are traversed for the following reasons. The Examiner's requirement regarding claims 24 and 25 is erroneous. Claims 24 and 25 respectively depend from claims 22 and 23 and therefore cover a different combination of limitations and are not substantial duplicates. If the Examiner persists in this ground of objection, it is requested that he clarify how, with the different dependencies noted above, claims 24 and 25 are substantial duplicates.

Claims 26 and 27 have been stated to be substantial duplicates. However, the same response regarding claims 24 and 25 is appropriate regarding claims 26 and 27.

Similarly, the remaining objections regarding claims 28-37 are erroneous since different dependencies are involved.

Claims 22-47 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claim 22 has been amended to address the matters noted by the Examiner. Specifically, claim 22 and claims dependent therefrom now recite an assembly of a ground plane and a semiconductor chip. The explanation of the invention in the first paragraph of the Remarks correlates the above elements of the disclosure with the claimed subject matter which demonstrates the support for the claimed invention in the specification.

The claimed "supporting member" is described in the specification as the interposer 4 which can be seen as supporting the assembly of the chip 1, insulator 2 and conductive glue 3 and metallic layer 5.

The Examiner has questioned how the via can be electrically coupled in series with the second capacitor point. As described above, this is shown in Fig. 1 from the direction in which current flows from the chip 1 through the capacitor formed by the internal wiring of the chip, dielectric layer 2 and the electrically conductive glue 3, through the metallic layer 5, the vias 7 and down through the printed circuit board 10.

The Examiner questions, how can "the second capacitor plate" at line 9 comprise a layer of conductive glue? The answer to this question is that the specification describes it as a capacitor plate. See paragraph 17 of the specification.

Claims 26 and 27 stand rejected as being indefinite based upon the Examiner's statement that it is "not clear regarding how can the dielectric layer be an integral part of the chip and at the same time cover an entire surface of the chip". These claims now recite the dielectric layer is an outer surface of the chip facing the supporting member.

Claims 28 and 29 are rejected as being unclear premised on "how can a 'dielectric layer' comprise 'silicon oxide', if 'silicon oxide' is a semiconductor? The response to the Examiner's question is that silicon oxide is an insulator and as is well know, dielectric layers are insulators. The Examiner's statement regarding silicon oxide as a semiconductor is not understood and silicon oxide as a semiconductor is not recited in the claims. The Examiner is incorrect in construing claim 28 as reciting the dielectric layer is a semiconductor. In this regard, paragraph [0016] of the Substitute Specification states that "[t]ypically, this layer 2 is an integrally formed layer comprising an oxide of the semiconductor material, i.e. silicon dioxide if the chip is made from silicon." Accordingly, it is submitted that claims 28 and 29 are supported by the specification and are definite.

Claims 30-37 have been amended to recite that the second capacitor plate comprises a metallic layer on the supporting member which electrically contacts

the layer of electrically conductive glue as illustrated in Fig. 1. Accordingly, it is submitted that claims 30-37 are definite.

Claim 48 has been amended to recite a method of assembly of a ground plane and a semiconductor chip which clarifies the nature of the invention.

Claims 22-48 stand rejected under 35 U.S.C. §103 as being unpatentable over EP 0630176 A1 (Blaupunkt) in view of United States Patent 5,741,729 (Selna). This ground of rejection is traversed for the following reasons.

Section 11 of the Office Action indicates as follows:

> Regarding the argument that EP 630,176 does not disclose: "a conductive glue" but rather a: "thermally conductive glue". It is pointed out that reference number 2 is disclosing a **conductive** glue, and independent claims 22 and 48 recite: "a layer of **conductive** glue", thus the claimed invention does not distinguishes over the prior art.

It is therefore seen that the Examiner is relying upon the teachings of Blaupunkt regarding thermally conductive glue.

Independent claim 22 recites an assembly of a ground plane and a semiconductor chip comprising at least one first capacitor plate provided within the semiconductor chip, and at least one second capacitor plate, the first and second capacitor plates being separated by a dielectric layer and capacitively coupled to each other via the dielectric layer, and the ground plane comprising at least one first conducting member and at least one electrically conductive via extending through a supporting member of the semiconductor chip and electrically coupled in series with the second capacitor plate; and wherein the second capacitor plate comprises a layer of electrically conductive glue which

attaches the ground plane to the semiconductor chip"; and claim 48 recites, a method of assembly of a ground plane and a semiconductor chip mounted on a supporting member of a chip containing a first capacitor plate and a dielectric coating, comprising providing the ground plane on a metal covered area on the surface of the supporting member, providing vias electrically connected to the metal covered area and extending therefrom through the supporting member to the opposite side thereof, connecting in parallel at least two of the vias which provide an inductance and are coupled to the ground plane, and using an electrically conductive glue between the chip and the metal covered area to attach the metal covered area to the chip. The combination of Blaupunkt and Selna does not meet the subject matter of the claims 22 and 48 including the electrically conductive glue and the associated limitations. The Examiner apparently tacitly understands this point by the statement reproduced above with regard to Section 11 of the Office Action by his statement that "the claimed invention does not distinguishes (sic) over the prior art".

The currently cited version of Blaupunkt is understood to be substantively identical to the previously cited EP 0 630 176 B1 in which it was pointed out in the first full paragraph on page 9 of the December 21, 2002 Amendment that glue 2 was thermally conductive. Accordingly, there is no teaching in the record regarding the electrically conductive glue in association with the other claim limitations. Therefore, even if the proposed combination of Blaupunkt and Selna was made, the subject matter of claims 24-48 would not be achieved.

Moreover, there is no basis why a person of ordinary skill in the art would make the proposed combination based on Examiner's reasoning that Selna would help "maintain the current flow in the package end reducing ground bounce and reducing IC signal delay time". This motivational basis is not suggested by either of the cited references. Accordingly, the motivation to combine the references does not appear to be fairly suggested by the prior art premised upon the Examiner's reasoning involving current flow, reducing ground bounce and IC signal delay. If the Examiner continues with the proposed combination, it is requested that he clarify the record regarding where the maintaining of current flow in the package and reducing ground bounce and reducing IC signal delay time would be understood by a person of ordinary skill in the art as a motivational basis to make the proposed combination.

Claim 49 stands rejected under 35 U.S.C. §103 as being unpatentable over Blaupunkt in view of United States Patent 4,954,179 (Jedlicka et al). Claim 49 defines a semiconductor chip package comprising a semiconductor chip containing a first capacitor plate and a dielectric coating and a supporting member, the supporting member comprising at least one metal covered area which is a ground plane and at least one electrically conductive via extending from the metal covered area through the supporting member which provides an inductance and are coupled to the ground plane, and wherein the chip is adhered to the supporting member by means of an electrically conductive glue and the

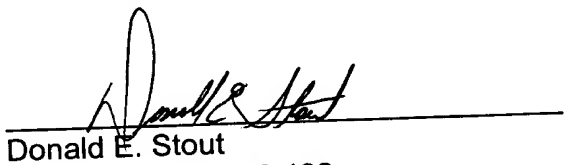
electrically conductive glue is in electrical contact with a metal covered area and wherein the electrically conductive glue is a second capacitor plate and the first and second capacitor plates in the dielectric form a capacitor and the capacitor and inductance are a series circuit coupling the capacitance to ground. This subject matter has no counterpart in a combination of Blaupunkt in view of Jedlicka et al. There is no basis why a person of ordinary skill in the art would be led to modify the teachings of Blaupunkt and Jedlicka et al to arrive at the subject matter of claim 49.

In view of the foregoing amendments and remarks, it is submitted that claims 22-49 are in condition for allowance.

To the extent necessary, Applicants petition for an extension of time under 37 C.F.R. §1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (612.38837X00) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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MARKED VERSION SHOWING CHANGES MADE ACCOMPANYING RULE 116 AMENDMENT

IN THE SPECIFICATION:

Please replace the following paragraphs:

[0002] In all analog circuit designs it is desirable to have a ground that is as close to 0 volts AC as possible. Normally circuit design assumes that ground nodes do not carry any AC-voltage. If a ground node, contrary to this assumption, does carry an AC-voltage, this may lead to unpredictable behavior, e.g. increased noise, distortion or even instability. The root cause of this is that all conductors have a non-zero impedance. This means that when a ground node has to source or sink a current there will be a voltage drop between the ground node and the actual ground point. This effect is much more pronounced in RF-circuits because the inductive nature of the impedance.

[0003] In integrated circuits the ground point of the die (semiconductor chip) is connected to the exterior via a bonding wire connected between the die and the interposer (or leadframe). The impedance of the bonding wire is important at RF-frequencies, and this makes it difficult to realize a proper ground node on the die. If the die is made bigger in order to make the bonding wire shorter, this only moves the

problem from the bonding wire to the die because the conductor on the die has to be longer.

[0004] Several solutions have been proposed to solve this problem. One is to make the C-package very small and the bonding wires short. This solution has several drawbacks. It is only viable for small scale integration circuits. In large scale integration circuits the die is larger and the ground conductors on the die are correspondingly longer. ~~And even~~ Moreover for small scale integrated circuits making the bonding wires short only reduces the problem, but does not solve it.

[0009] In general terms according to the present invention the problem is solved by placing a metal-covered area on the interposer under the die. Vias on the interposer connect the area to the underside of the interposer. The die is glued to the area with electrically conducting glue. A capacitor is thus formed, the capacitor being formed by the die substrate, the oxide layer on the underside of the die, and the conductive plate on the interposer. By making all other associated impedances as small as possible, e.g. by connecting the metal-plate on the top side of the interposer to the bottom side by using multiple vias in parallel, the resulting impedance can be made very low, less than 20 Ohms, even at high frequencies. If the integrated circuit has a well defined working frequency, the RF-ground plane can be tuned to that frequency by choosing the dimensions of the associated conductors, and thus the inductance of the conductors, so that the resonant frequency of the inductance and capacitor coincides with the

working frequency. The impedance at said working frequency can be made extremely low, close to 2 Ohms.

[0017] The chip I is glued to an insulating interposer 4 carrying a conductive area 5. Typically the conductive area 5 is a metal covered area. The glue 3 is electrically conductive and serves not only the purpose of adhering the chip 1 to the interposer 4, but also forms a capacitor plate, capacitively coupled to internal parts (not shown) of the chip, but insulated therefrom by the insulating layer 2.

[0020] In this respect it should be noted that even though the metal coated area in the embodiments shown corresponds largely to the dimensions of the chip this is not a prerequisite for the invention to work. Instead, because the electrically conductive glue defines the capacitor plate vis-à-vis the internal parts, it is in principle sufficient to contact the glue 3 to the vias 7.

[0023] The capacitance value has been found to be approximately ten times higher when using electrically conductive glue as compared to non-conductive glue.

[0024] Thus without the electrically conductive glue 3 the capacitance value becomes both smaller and less predictable.

[0028] It is known that any conducting member exhibits an inductance. Thus, ~~an~~ a LC series circuit is formed by the capacitance provided between internal parts of the chip and the conductive glue 3 separated by the dielectric layer 2, and the

inductance provided by the vias 7. If the chip has a well defined working frequency, the number of vias may be chosen, so that the series resonant frequency of the inductance provided by the vias and the aforementioned capacitance, approximately matches the working frequency of the chip. In this way an extremely low ground impedance of 2 Ohms or less, can be achieved.

IN THE CLAIMS:

Original Claims 1-21 were previously cancelled and new claims 22-49 were previously added. The pending claims are 22-49 as follows:

22. (~~New~~Currently Amended) An assembly of a ground plane ~~for~~ and a semiconductor chip ~~for mounting on a supporting member in a chip package~~, comprising:

at least one first capacitor plate provided within the semiconductor chip, and at least one second capacitor plate, the first and second capacitor plates being separated by a dielectric layer and capacitively coupled to each other via the dielectric layer, and the ground plane comprising at least one first conducting member~~, including~~ and at least one electrically conducting via extending through ~~the~~ a supporting member of the semiconductor chip and electrically coupled in series with the second capacitor plate; and wherein

the second capacitor plate comprises a layer of electrically conductive glue which attaches the ground plane to the semiconductor chip.

23. (~~New~~Currently Amended) ~~A ground plane~~ An assembly according to claim 22, wherein:

a resonant frequency of the capacitance provided by the first capacitor plate and the second capacitor plate, and an inductance provided by the at least one first conducting member, is approximately equal to an intended working frequency of the chip.

24. (~~New~~Currently Amended) ~~A ground plane~~ An assembly according to claim 22, wherein:

the dielectric layer is an integral part of the chip.

25. (~~New~~Currently Amended) ~~A ground plane~~ An assembly according to claim 23, wherein:

the dielectric layer is an integral part of the chip.

26. (~~New~~Currently Amended) ~~A ground plane~~ An assembly according to claim 24, wherein:

the dielectric layer ~~covers an entire~~ is an outer surface of the chip facing the supporting member.

27. (~~New~~Currently Amended) ~~A ground plane~~ An assembly according to claim 25, wherein:

the dielectric layer ~~covers an entire~~ is an outer surface of the chip facing the supporting member.

28. (~~New~~Currently Amended) ~~A ground plane~~ An assembly according to claim 24, wherein:

the dielectric layer comprises silicon oxide.

29. (~~New~~Currently Amended) ~~A ground plane~~ An assembly according to claim 25, wherein:

the dielectric layer comprises silicon oxide.

30. (~~New~~Currently Amended) ~~A ground plane~~ An assembly according to claim 22, wherein:

the second capacitor plate ~~is~~ comprises a metallic layer on the supporting member which electrically contacts the layer of electrically conductive glue.

31. (~~New~~Currently Amended) ~~A ground plane~~ An assembly according to claim 23, wherein:

the second capacitor plate ~~is~~ comprises a metallic layer on the supporting member which electrically contacts the layer of electrically conductive glue.

32. (~~New~~Currently Amended) ~~A ground plane~~ An assembly according to claim 23 wherein:

the second capacitor plate ~~is~~ comprises a metallic layer on the supporting member which electrically contacts the layer of electrically conductive glue.

33. (~~New~~Currently Amended) ~~A ground plane~~ An assembly according to claim 23, wherein:

the second capacitor plate ~~is~~ comprises a metallic layer on the supporting member which electrically contacts the layer of electrically conductive glue.

34. (~~New~~Currently Amended) ~~A ground plane~~ An assembly according to claim 23, wherein:

the second capacitor plate ~~is~~ comprises a metallic layer on the supporting member which electrically contacts the layer of electrically conductive glue.

35. (~~New~~Currently Amended) ~~A ground plane~~ An assembly according to claim 23, wherein:

the second capacitor plate ~~is~~ comprises a metallic layer on the supporting member which electrically contacts the layer of electrically conductive glue.

36. (~~New~~Currently Amended) ~~A ground plane~~ An assembly according to claim 23, wherein:

the second capacitor plate ~~is~~ comprises a metallic layer on the supporting member which electrically contacts the layer of electrically conductive glue.

37. (~~New~~Currently Amended) ~~A ground plane~~ An assembly according to claim 23, wherein:

the second capacitor plate ~~is~~ comprises a metallic layer on the supporting member which electrically contacts the layer of electrically conductive glue.

Claims 38-45 are cancelled without disclaimer or prejudice.

~~38.(New) A ground plane according to claim 30, wherein:~~

~~the layer of conductive glue is provided between the metallic layer and the dielectric layer.~~

~~39. (New) A ground plane according to claim 31, wherein:~~

~~the layer of conductive glue is provided between the metallic layer and the dielectric layer.~~

~~40. (New) A ground plane according to claim 32, wherein:~~

~~the layer of conductive glue is provided between the metallic layer and the dielectric layer.~~

~~41. (New) A ground plane according to claim 33, wherein:~~

~~the layer of conductive glue is provided between the metallic layer and the dielectric layer.~~

~~42. (New) A ground plane according to claim 34, wherein:~~

~~the layer of conductive glue is provided between the metallic layer and the dielectric layer.~~

~~43. (New) A ground plane according to claim 35, wherein:~~

~~the layer of conductive glue is provided between the metallic layer and the dielectric layer.~~

~~44. (New) A ground plane according to claim 36, wherein:~~

~~the layer of conductive glue is provided between the metallic layer and the dielectric layer.~~

~~45. (New) A ground plane according to claim 37, wherein:~~

~~the layer of conductive glue is provided between the metallic layer and the dielectric layer.~~

46. (~~New~~Currently Amended) ~~A ground plane~~ An assembly according to claim 22, wherein:

the at least one electrically conducting via extending through the supporting member is directly connected to the second capacitor plate.

47. (~~New~~Currently Amended) ~~A ground plane~~ An assembly according to claim 30, wherein:

the vias and the metallic layer are integrally formed from a same metal.

48. (~~New~~Currently Amended) A method ~~for providing~~ of assembly of a ground plane ~~for~~ and a semiconductor chip mounted on a supporting member ~~in~~ of a chip ~~package~~ containing a first capacitor plate and a dielectric coating, comprising providing ~~a~~ the ground plane on a metal covered area on ~~the~~ a surface of the supporting member, providing vias electrically connected to the metal covered area and extending therefrom through the supporting member to the opposite side thereof, connecting in parallel at least two of the vias which provide an inductance and are coupled to the ground plane, and using an electrically conductive glue between the chip and the metal covered area to attach the metal covered area to the chip.

49. (~~New~~Currently Amended) A semiconductor chip package comprising:

a semiconductor chip containing a first capacitor plate and a dielectric coating and a supporting member, the supporting member comprising at least one metal covered area which is a ground plane and at least one electrically conductive via extending from the metal covered area through the supporting member which provides an inductance and are coupled to the ground plane, and wherein the chip is adhered to the supporting member by means of an electrically conductive glue and

the electrically conductive glue is in electrical contact with the metal covered area[.] and the electrically conductive glue is a second capacitor plate and the first and second capacitor plates and the dielectric form a capacitor and the capacitance and inductance comprise a series circuit coupling the capacitance to ground.